**IN THE CLAIMS**

All pending claims are listed below in revised format. Claims 4-6 and 10-31 are cancelled without prejudice to their subject matter. New claims 32-46 are added as indicated below. Claims 1-3, 7-9 and 32-46 remain in the application.

1. (Original) A method of using a transient voltage suppression device, comprising:

electrically coupling gate and drain terminals of a metal oxide semiconductor device;

clamping a forward voltage applied across the transient voltage suppression device to be substantially equal to a threshold potential of the metal oxide semiconductor device; and

clamping a reverse voltage applied across the transient voltage suppression device to be substantially equal to a barrier potential of the metal oxide semiconductor device.

2. (Original) The method of claim 1 wherein clamping the forward voltage comprises:

applying a first potential of a first polarity to the gate and drain terminals of the metal oxide semiconductor device; and

producing a first conductive state of the metal oxide semiconductor device with the first potential.

3. (Original) The method of claim 2 wherein clamping the reverse voltage comprises:

applying a second potential of a second polarity to the gate and drain terminals of the metal oxide semiconductor device; and

producing a second conductive state of the metal oxide semiconductor device with the second potential.

Please cancel claims 4-6 without prejudice to their subject matter.

7. (Original) A method of using a transient voltage suppression device, comprising:

electrically coupling gate and drain terminals of first and second metal oxide semiconductor devices;

clamping a forward voltage applied across the transient voltage suppression device to be substantially equal to a first threshold potential of the first metal oxide semiconductor device; and

clamping a reverse voltage applied across the transient voltage suppression device to be substantially equal to a second threshold potential of the second metal oxide semiconductor device.

8. (Original) The method of claim 7 wherein clamping the forward voltage comprises:

applying a first potential of a first polarity to the gate and drain terminals of the first metal oxide semiconductor device; and

producing a first conductive state of the first metal oxide semiconductor device with the first potential.

9. (Original) The method of claim 8 wherein clamping the reverse voltage comprises:

applying a second potential of a second polarity to the gate and drain terminals of the second metal oxide semiconductor device; and

producing a second conductive state of the second metal oxide semiconductor device with the second potential.

Please cancel claims 10-31 without prejudice to their subject matter. Add new claims 32-43 as follows.

32. (New) A semiconductor device for suppressing an external transient voltage, comprising an insulated gate bipolar transistor (IGBT) having a gate terminal and a first conduction terminal coupled to receive the external transient voltage, and a second conduction terminal to shunt a surge current flowing through the first conduction terminal in response to the external transient voltage exceeding a predetermined level.

33. (New) The semiconductor device of claim 32, further comprising a semiconductor substrate having a top surface for forming the first conduction terminal and the gate terminal of the IGBT.

34. (New) The semiconductor device of claim 33, wherein the semiconductor substrate includes:

a body region of a first conductivity type for inverting to form a channel of the IGBT;

an emitter region formed at the first surface for receiving the surge current from the first conduction terminal; and

a drift region having a second conductivity type and coupled to the channel for conducting the surge current.

35. (New) The semiconductor device of claim 34, wherein the semiconductor substrate further includes a collector region of the first conductivity type formed adjacent to the drift region for routing the surge current between the drift region and the second conduction terminal.

36. (New) The semiconductor device of claim 35, wherein the collector region is formed on the top surface of the semiconductor substrate.

37. (New) The semiconductor device of claim 35, wherein the semiconductor substrate has a bottom surface for forming the collector region and the second conduction terminal.

38. (New) The semiconductor device of claim 37, further comprising a semiconductor package having a die flag for mounting the semiconductor substrate, wherein the collector region is electrically coupled to the die flag for routing the surge current to an external node.

39. (New) The semiconductor device of claim 38, wherein the semiconductor package further includes a bonding wire coupled between the gate terminal and the die flag.

40. (New) The semiconductor device of claim 37, further comprising a collection region of the first conductivity type that is coupled to the first conduction terminal and formed at the top surface for collecting minority carriers injected from the collector region.

41. (New) The semiconductor device of claim 34, further comprising first and second diodes coupled in a back to back fashion between the gate and first conduction terminals.

42. (New) The semiconductor device of claim 41, wherein the first and second diodes are formed in a semiconductor layer disposed on the top surface of the semiconductor substrate.

43. (New) The semiconductor device of claim 42, wherein a region of the semiconductor layer overlies the channel to form the gate terminal of the IGBT.

44. (New) The semiconductor device of claim 42, wherein the semiconductor layer is formed with polycrystalline silicon.

45. (New) The semiconductor device of claim 44, wherein the external transient voltage turns on the IGBT to conduct the surge current between the first and second conduction terminals at a level greater than about five amperes.

46. (New) The semiconductor device of claim 45, wherein the IGBT limits a magnitude of the external voltage transient to a value less than about five volts.